#19C/5-19-02 V. Jones

.IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Daniel L. Auclair, Jeffrey Craig, John S. Mangan, Robert D. Norman, Daniel C. Guterman and Sanjay Mehrotra		
Title:	Soft Errors Handling in EEprom Devices		
Serial No.:	08/908,265	Filing Date:	August 7, 1997
Examiner:	E. Moise	Group Art Unit:	2133
Docket No.:	M-10202-3C US		

San Francisco, California
May 9, 2002

BOX AFTER FINAL
COMMISSIONER FOR PATENTS
Washington, D. C. 20231

AMENDMENT AFTER FINAL

Dear Sir:

Responsive to the Official Action mailed on February 12, 2002, setting a response period expiring on May 12, 2002, applicant responds to the Official Action as follows:

In the Claims

Please add the following new claims:

--45. A method of operating a memory device having a plurality of memory cells, comprising:

generating a first read voltage;

applying said first read voltage to a terminal of a first cell of the plurality of memory cells;

generating a first read result in response to said applying said first read voltage;

generating a second read voltage;

applying said second read voltage to said terminal of said first cell;

generating a second read result in response to said applying said first read voltage; and

determining from said first and second read results whether data storage of the memory device is deteriorated.

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